IN THE CLAIMS

Please cancel claim 2 without prejudice.

Please amend claims 1 and 5-6 as indicated below.

1. (Currently Amended) A method for current calibration of a plurality of I/O cells of an integrated circuit (IC) comprising:

setting a global control value;

providing the global value to the plurality of I/O cells to cause each of the plurality of I/O cells to output a logic voltage at a corresponding output pad; and

for each I/O cell:

feeding back the logic voltage at the corresponding output pad to a comparator;

comparing the logic voltage at the corresponding output pad with a reference voltage; and

sinking current at the corresponding output pad based on result of the comparing, sinking current at the output pad including sinking current at the corresponding output pad until the logic voltage at the corresponding output pad and the reference voltage are substantially equal.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein sinking current at the corresponding output pad comprises:

enabling additional driver bits to sink more current at the corresponding output pad if the logic voltage is higher than the reference voltage; and

disabling additional driver bits to sink less current at the corresponding output pad if the logic voltage is lower than the reference voltage.

4. (Previously Presented) The method of claim 3, wherein sinking current at the corresponding output pad comprises modifying a local value stored in a register device associated with a corresponding I/O cell based on the comparing of the logic voltage and the reference voltage.

5. (Currently Amended) ~~The method of claim 4~~ A method for current calibration of a plurality of I/O cells of an integrated circuit (IC) comprising:

setting a global control value;

providing the global value to the plurality of I/O cells to cause each of the plurality of I/O cells to output a logic voltage at a corresponding output pad; and

for each I/O cell:

feeding back the logic voltage at the corresponding output pad to a comparator;

comparing the logic voltage at the corresponding output pad with a reference voltage; and

sinking current at the corresponding output pad based on result of the comparing, sinking current at the corresponding output pad including

enabling additional driver bits to sink more current at the corresponding output pad if the logic voltage is higher than the reference voltage,

disabling additional driver bits to sink less current at the corresponding output pad if the logic voltage is lower than the reference voltage, and

modifying a local value stored in a register device associated with a corresponding I/O cell based on the comparing of the logic voltage and the reference voltage, wherein the register device comprises a counter and the local value is modified by incrementing or decrementing the local value.

6. (Currently Amended) A method comprising:

setting a global control value provided to a plurality of I/O cells to cause each of the plurality of I/O cells to output a logic voltage on a corresponding output pad;

then, for each of the plurality of I/O cells:

feeding back the logic voltage at the corresponding output pad to a comparator;

~~setting a local value in a register device associated with the I/O cell in response to the global control value;~~

comparing the logic voltage with a reference voltage; and

setting a local value in a register device associated with a corresponding I/O cell in response to the global control value and result of the comparing of the logic voltage and the reference voltage, setting a local value in a register device including sinking a current at the corresponding IO cell until the logic voltage at the corresponding IO cell and the reference voltage are substantially equal.

7. (Previously Presented) The method of claim 6, further comprising enabling additional driver bits to modify the local value in the register device associated with the corresponding I/O cell in response to the comparison of the logic voltage and the reference voltage to sink more current at the corresponding output pad.

8. (Previously Presented) The method of claim 6, further comprising disabling additional driver bits to modify the local value in the register device associated with the I/O cell in response to the comparison of the logic voltage and the reference voltage to sink less current at the corresponding output pad.

9. (Previously Presented) The method of claim 4, further comprising shifting at least one of "1" and "0" into the register device to modify the local value.